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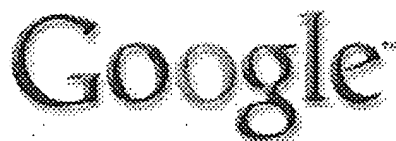
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☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**1 Dynamic and transparent binary translation***Gschwind, M.; Altman, E.R.; Sathaye, S.; Ledak, P.; Appenzeller, D.;*  
Computer, Volume: 33, Issue: 3, March 2000  
Pages: 54 - 59[\[Abstract\]](#)   [\[PDF Full-Text \(293 KB\)\]](#)   **IEEE JNL****2 Dynamic binary translation for accumulator-oriented architectures***Ho-Seop Kim; Smith, J.E.;*  
Code Generation and Optimization, 2003. CGO 2003. International Symposium on, 23-26 March 2003  
Pages: 25 - 35[\[Abstract\]](#)   [\[PDF Full-Text \(362 KB\)\]](#)   **IEEE CNF**


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### Web-Based Simulators for DSPs and Microcontrollers

[www.ece.utexas.edu/~bevans/projects/webtools/web\\_simulators.html](http://www.ece.utexas.edu/~bevans/projects/webtools/web_simulators.html) - [Similar pages](#)

### [PDF] Randomized Instruction Set Emulation to Disrupt Binary Code ...

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... using Valgrind [36] for the Intel x86 **architecture**. ... contains a complete x86-to- x86 **binary translator**. ... and that a randomized **instruction set** prevents injected ...

[www.cs.unm.edu/~forrest/publications/p315-barrantes.pdf](http://www.cs.unm.edu/~forrest/publications/p315-barrantes.pdf) - [Similar pages](#)

### [PDF] Randomized instruction set emulation to disrupt binary code ...

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... Valgrind [23] for the Intel x86 **architecture**. ... it contains a complete binary-to-binary **translator**. ... code injections unaware of the effective **instruction set**. ...

[www.cs.unm.edu/~darko/papers/tr-cs-2003-10-rise.pdf](http://www.cs.unm.edu/~darko/papers/tr-cs-2003-10-rise.pdf) - [Similar pages](#)
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### Dino A. Dai Zovi

... based on the open-source Valgrind x86-to-x86 **binary translator**. ... consequences of the dense x86 **instruction set** on the ... of native or foreign **architecture** binaries ...

[www.theta44.org/main.html](http://www.theta44.org/main.html) - 12k - [Cached](#) - [Similar pages](#)

### [PS] CS 497yyz Project Report: LLVA-emu

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... 2003 LLVA-emu **command line**: "" **Kernel command line**: WARNING: trap ... A Low-level Virtual **Instruction Set Architecture**. ... FXI32: A profile-directed **binary translator**. ...

[llvm.cs.uiuc.edu/ProjectsWithLLVM/2003-Fall-CS497YYZ-LLVA-emu.ps](http://llvm.cs.uiuc.edu/ProjectsWithLLVM/2003-Fall-CS497YYZ-LLVA-emu.ps) - [Similar pages](#)

### [PDF] CS 497yyz Project Report: LLVA-emu

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... LLVA-emu **command line**: "" **Kernel command line**: WARNING: trap init ... A Low-level Virtual **Instruction Set Architecture**. ... FXI32: A profile-directed **binary translator**. ...

[llvm.cs.uiuc.edu/ProjectsWithLLVM/2003-Fall-CS497YYZ-LLVA-emu.pdf](http://llvm.cs.uiuc.edu/ProjectsWithLLVM/2003-Fall-CS497YYZ-LLVA-emu.pdf) - [Similar pages](#)

### Citations: The New Jersey machine-code toolkit - Ramsey, Fern' ...

... In a **binary translator**, this information ... from concise specifications of **instruction set** formats. ... to read several different machine **architecture** assembly files ...

[citeseer.nj.nec.com/context/10363/6551](http://citeseer.nj.nec.com/context/10363/6551) - 39k - [Cached](#) - [Similar pages](#)

### Citations: Using and Porting GNU CC - Stallman (ResearchIndex)

... file (eg in a **binary translator**'s frontend ... nML formalism models the **instruction set architecture** of a machine but ... code for the MIPS **architecture** (a DECStation ...

[citeseer.nj.nec.com/context/10367/0](http://citeseer.nj.nec.com/context/10367/0) - 32k - [Cached](#) - [Similar pages](#)

### [PDF] HP Caliper – An Architecture for Performance Analysis Tools

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... by the IA-64 runtime software **architecture** [10 ... A Resourceable and Retargetable **Binary Translator**", University of ... Shade: A Fast **Instruction-Set** Simulator for ...

[www.usenix.org/events/osdi2000/wiess2000/full\\_papers/hundt/hundt.pdf](http://www.usenix.org/events/osdi2000/wiess2000/full_papers/hundt/hundt.pdf) - [Similar pages](#)

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... IA-64 runtime software **architecture** [10 ... A Resourceable and Retargetable **Binary Translator**",


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### Citations: An **out-of-order** execution technique for runtime binary ...

... Work Le [11] presents a runtime **binary translator** which allows ... An **out-of-order** execution technique for runtime binary ... which must be moved **in order** to correctly ...

[citeseer.nj.nec.com/context/918333/0](http://citeseer.nj.nec.com/context/918333/0) - 21k - [Cached](#) - [Similar pages](#)

### Dynamo: A Transparent Dynamic Optimization System - Vasanth ...

... more challenging situation, **in order** to emphasize ... 1997 8 a profile-directed **binary translator** (context) - Chernoff ... Alpha processor with **out-of-order** e.. (context ...

[citeseer.nj.nec.com/bala00dynamo.html](http://citeseer.nj.nec.com/bala00dynamo.html) - 25k - [Cached](#) - [Similar pages](#)

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### [PDF] SCISM IA-32 Binary Translator

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... over- all architecture of the **binary translator** and describes ... original program, allowing for **out-of-order** issue. ... **In order** to achieve this, the com- pounding ...

[ce.et.tudelft.nl/publicationfiles/825\\_425\\_koukourechkov.pdf](http://ce.et.tudelft.nl/publicationfiles/825_425_koukourechkov.pdf) - [Similar pages](#)

### Dynamo

... latter, more challenging situation, **in order** to emphasize ... FX!32: a profile-directed **binary translator**. ... a superscalar Alpha processor with **out-of-order** execution ...

[portal.acm.org/citation.cfm?id=349303&dl=ACM&coll=portal&CFID=11111111&CFTOKEN=2222222](http://portal.acm.org/citation.cfm?id=349303&dl=ACM&coll=portal&CFID=11111111&CFTOKEN=2222222) - [Similar pages](#)

### [PDF] A Dynamic Binary Translation Approach to Architectural Simulation

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... in the translated code, allowing an **out-of-order** processor model ... We make this requirement **in order** to simplify the ... of our dynamic **binary translator**, which has ...

[www.cs.wisc.edu/~cain/pubs/wbt\\_cain.pdf](http://www.cs.wisc.edu/~cain/pubs/wbt_cain.pdf) - [Similar pages](#)

### [PPT] IPF Base OS Implementation

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... **Binary translator**. HP Services will be prepared to assist. ... Instructions completed **in order** issued. Limited use of pipelines. ... **Out of order** instruction completion. ...

[www.canacu.org/ts-0008.ppt](http://www.canacu.org/ts-0008.ppt) - [Similar pages](#)

### The Great CPU List. Section 5

... the tracking of these instructions, **in-order** groups of ... Instructions that can't execute **out of order** form a group ... Windows NT) using a **binary translator**, as well ...

[www3.sk.sympatico.ca/bayko/cpu5.html](http://www3.sk.sympatico.ca/bayko/cpu5.html) - 35k - [Cached](#) - [Similar pages](#)

### High Performance Computing Group - Industrial Affiliates Program

... managed cache with two modules **in order** to exploit ... Dixie is both a **binary translator** and a binary ... a vector unit to a current **out-of-order** superscalar processor ...

[research.ac.upc.es/CAP/affiliates/projects/micro/recent.html](http://research.ac.upc.es/CAP/affiliates/projects/micro/recent.html) - 12k - [Cached](#) - [Similar pages](#)

### [PDF] Binary translation : Classification of emulators

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... can be pipelined and individually scheduled **out of order**. ? ... Furthermore, **in order** to gain any momentum ... binary acceleration: A **binary translator** that translates ...

[www.liacs.nl/~atijms/bintrans.pdf](http://www.liacs.nl/~atijms/bintrans.pdf) - [Similar pages](#)

### [PDF] Register Liveness Analysis for Optimizing Dynamic Binary ...